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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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David Presley Wallace

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EXAMINER

LOUIE, OSCAR A

ART UNIT

PAPER NUMBER

2136

NOTIFICATION DATE

DELIVERY MODE

03/18/2008

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 10/764,770	Applicant(s) WALLACE ET AL.	
	Examiner OSCAR A. LOUIE	Art Unit 2136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 December 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2-5 and 7-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 2-5 & 7-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This final action is in response to the amendment filed on 12/12/2007. In light of the applicant's amendments and remarks, the examiner hereby withdraws his previous 35 U.S.C. 112 2nd paragraph rejection regarding Claims 5-8 and specification objection. The examiner acknowledges that Claims 1 & 6 have been cancelled. Claims 2-5 & 7-9 are pending and have been considered as follows.

Claim Objections

1. Claims 2, 5, 7, & 8 are objected to because of the following informalities:
 - Claim 2 lines 1-2 recite "For use with" which should be "...In..."
 - Claim 5 line 1 recites "For use with" which should be "...In..."
 - Claim 5 line 4 recites "for" which should be "...configured to..."
 - Claim 5 line 11 recites "operative" which should be "...configured to..."
 - Claim 5 line 14 recites "which is operative" which should be "...configured..."
 - Claim 7 line 5 recites "for" which should be "...configured to..."
 - Claim 7 line 8 recites "adapted" which should be "...configured..."
 - Claim 7 lines 10, 16, & 18 recite "operative" which should be "...configured..."
 - Claim 8 line 2 recites "operative" which should be "...configured..."

Appropriate correction is required.

Examiner's Note

In light of the applicant's remarks and the applicant's specification on pages 3 & 4 regarding the definition of an "arrangement," the examiner has interpreted Claims 5 & 7 and their dependents as an apparatus for the considerations below.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 2-5 & 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Sutherland (US-6292898-B1).

Claim 2:

Sutherland discloses for use with an electronic signal processing apparatus containing a security key memory which stores a security key that enables a user to operate said electronic signal processing apparatus, a method of preventing access to said security key in the event of a compromise in the integrity of a housing for said security key memory comprising,

- "(a) monitoring the integrity of said housing" (i.e. "A detector 303 is adapted, as described in more detail below, to detect an intrusion into the secure environment") [column 5 lines 52-53];
- "(b) in response to step (a) detecting said compromise in the integrity of said housing" (i.e. "detect an intrusion into the secure environment") [column 5 lines 52-53];

- “changing the contents of said security key memory so as to effectively remove said security key from said security key memory” (i.e. “electrical current is either supplied from a reference voltage generator 305 to the volatile data storage device 301 or sourced to the reference voltage generator 305 from the volatile data storage device 301 to effect erasure of data stored in the volatile data storage device”) [column 5 lines 59-63];
- “wherein step (a) comprises storing, in a single-bit storage device, a single bit representative of a prescribed power supply state of said security key memory” (i.e. “volatile data storage devices typically require maintenance of two voltage levels (data retention voltages) within the volatile data storage device to enable one of two distinct values to be stored in each memory cell of the volatile data storage device, data being stored in the volatile data storage device by selectively storing one of the two distinct values in particular memory cells”) [column 6 lines 9-16];
- “changing the bit state, of said single-bit storage device in response to said compromise in the integrity of said housing for said memory” (i.e. “the clamp 304 supplies current to or from the reference voltage generator 305 from or to, respectively, one or more such designated input nodes of the volatile data storage device 301 so that the voltages at the designated input nodes become equal”) [column 6 lines 18-22].

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Claim 3:

Sutherland discloses for use with an electronic signal processing apparatus containing a security key memory which stores a security key that enables a user to operate said electronic signal processing apparatus, a method of preventing access to said security key in the event of a compromise in the integrity of a housing for said security key memory, as in Claim 2 above, further comprising,

- “wherein step (b) comprises in response to step (a) detecting a change in the bit state of said single-bit storage device” (i.e. “When the voltages at the designated input nodes become equal, the data retention voltages in the volatile data storage device 301 become equal as well”) [column 6 lines 25-27];
- “changing the contents of said security key memory so as to effectively remove said security key from said security key memory” (i.e. “Since the data retention voltages are equal, each memory cell of the volatile data storage device 301 stores the same value and, thus, all of the data stored in the volatile data storage device 301 is effectively erased”) [column 6 lines 27-31].

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Claim 4:

Sutherland discloses for use with an electronic signal processing apparatus containing a security key memory which stores a security key that enables a user to operate said electronic signal processing apparatus, a method of preventing access to said security key in the event of a compromise in the integrity of a housing for said security key memory, as in Claim 2 above, further comprising,

- “wherein step (a) comprises coupling a switch, having a closure state dependent upon the integrity of said housing, to said single-bit storage device” (i.e. “the clamp 304 supplies current to or from the reference voltage generator 305 from or to, respectively, one or more such designated input nodes of the volatile data storage device 301 so that the voltages at the designated input nodes become equal”) [column 6 lines 18-22];
- “in response to said compromise in the integrity of said housing, operating said switch, so as to change the bit state of said single-bit storage device” (i.e. “the clamp 304 supplies current to or from the reference voltage generator 305 from or to, respectively, one or more such designated input nodes of the volatile data storage device 301 so that the voltages at the designated input nodes become equal”) [column 6 lines 18-22].

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Claim 5:

Sutherland discloses for use with an electronic signal processing apparatus containing a security key memory in which is stored a security key that enables a user to operate said electronic signal processing apparatus, an arrangement for preventing access to said security key in the event of a compromise in the integrity of a housing for said security key memory comprising,

- “a single-bit storage device which is coupled to store a single bit representative of a prescribed power supply state of said security key memory” (i.e. “volatile data storage devices typically require maintenance of two voltage levels (data retention voltages) within the volatile data storage device to enable one of two distinct values to be stored in each memory cell of the volatile data storage device, data being stored in the volatile data storage device by selectively storing one of the two distinct values in particular memory cells”) [column 6 lines 9-16];
- “a switch, which is coupled to said single-bit storage device, and is operative to change the bit state thereof in response to said compromise in the integrity of said housing for said memory” (i.e. “the clamp 304 supplies current to or from the reference voltage generator 305 from or to, respectively, one or more such designated input nodes of the volatile data storage device 301 so that the voltages at the designated input nodes become equal”) [column 6 lines 18-22];
- “a control circuit, which is operative, in response to said change in the bit state of said single-bit storage device, to change the contents of said security key memory so as to effectively remove said security key from said security key memory” (i.e. “the clamp 304

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supplies current to or from the reference voltage generator 305 from or to, respectively, one or more such designated input nodes of the volatile data storage device 301 so that the voltages at the designated input nodes become equal”) [column 6 lines 18-22].

Claim 7:

Sutherland discloses in an electronic signal processing apparatus containing a security key memory, which stores a security key that enables a user to operate said electronic signal processing apparatus, an arrangement for preventing access to said security key in the event of a compromise in the integrity of a housing for said security key memory comprising,

- “an intrusion detection circuit that is adapted to monitor the integrity of said housing” (i.e. “A detector 303 is adapted, as described in more detail below, to detect an intrusion into the secure environment”) [column 5 lines 52-53];
- “a memory contents modification circuit that is operative, in response to said intrusion detection circuit detecting a compromise in the integrity of said housing, to modify the contents of said security key memory and thereby effectively remove said security key from said security key memory” (i.e. “electrical current is either supplied from a reference voltage generator 305 to the volatile data storage device 301 or sourced to the reference voltage generator 305 from the volatile data storage device 301 to effect erasure of data stored in the volatile data storage device”) [column 5 lines 59-63];
- “said intrusion detection circuit includes a single-bit storage device that is operative to store a single bit representative of a prescribed power supply state of said security key memory” (i.e. “volatile data storage devices typically require maintenance of two voltage levels (data retention voltages) within the volatile data storage device to enable one of

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two distinct values to be stored in each memory cell of the volatile data storage device, data being stored in the volatile data storage device by selectively storing one of the two distinct values in particular memory cells”) [column 6 lines 9-16];

- “a switch that is operative to change the bit state of said single-bit storage device in response to said compromise in the integrity of said housing for said memory” (i.e. “the clamp 304 supplies current to or from the reference voltage generator 305 from or to, respectively, one or more such designated input nodes of the volatile data storage device 301 so that the voltages at the designated input nodes become equal”) [column 6 lines 18-22].

Claim 8:

Sutherland discloses in an electronic signal processing apparatus containing a security key memory, which stores a security key that enables a user to operate said electronic signal processing apparatus, an arrangement for preventing access to said security key in the event of a compromise in the integrity of a housing for said security key memory, as in Claim 7 above, further comprising,

- “said memory contents modification circuit is operative, in response to a change in the bit state of said single-bit storage device, to change the contents of said security key memory so as to effectively remove said security key from said security key memory” (i.e. “Since the data retention voltages are equal, each memory cell of the volatile data storage device 301 stores the same value and, thus, all of the data stored in the volatile data storage device 301 is effectively erased”) [column 6 lines 27-31].

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Claim 9

Sutherland discloses in an electronic signal processing apparatus containing a security key memory, which stores a security key that enables a user to operate said electronic signal processing apparatus, an arrangement for preventing access to said security key in the event of a compromise in the integrity of a housing for said security key memory, as in Claim 8 above, further comprising,

- “said switch has a closure state dependent upon the integrity of said housing” (i.e. “the clamp 304 supplies current to or from the reference voltage generator 305 from or to, respectively, one or more such designated input nodes of the volatile data storage device 301 so that the voltages at the designated input nodes become equal”) [column 6 lines 18-22].

Response to Arguments

4. Applicant's arguments filed 12/12/2007 have been fully considered but they are not persuasive.

- The applicant's argument which states, “Sutherland makes no reference to a security key or a security key memory,” has been considered but is non-persuasive. The examiner considers the point of whether the memory is a security key memory to be immaterial of any novelty of the applicant's invention as claimed. Sutherland may not explicitly disclose a “security key memory,” but it is clear that the invention as disclosed by

Sutherland would be applicable to any type of memory where there is a need to wipe the contents of a memory in the event of an intrusion is detected in order to protect sensitive contents stored on said memory.

- The applicant's argument which states, "Sutherland makes no teaching whatsoever of "a single-bit storage device" which is now found in each of the independent claims. Further, Sutherland does not teach or suggest the use of the single-bit storage device in the manner claimed," has been considered but is non-persuasive. Sutherland discloses, "volatile data storage devices typically require maintenance of two voltage levels (data retention voltages) within the volatile data storage device to enable one of two distinct values to be stored in each memory cell of the volatile data storage device, data being stored in the volatile data storage device by selectively storing one of the two distinct values in particular memory cells") [column 6 lines 9-16], which is a single-bit storage device where the single bit determines a distinct voltage affecting whether the memory is to be wiped in the event of an intrusion detection.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Oscar Louie whose telephone number is 571-270-1684. The examiner can normally be reached Monday through Thursday from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nasser Moazzami, can be reached at 571-272-4195. The fax phone number for Formal or Official faxes to Technology Center 2100 is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

OAL
03/06/2008

/Nasser G Moazzami/
Supervisory Patent Examiner, Art Unit 2136

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